Amendments to the Drawings

The attached sheets of drawings include New Figs. 19 to 24.

Attachment: New Sheets

REMARKS

Applicant thanks the Examiner for careful consideration of this application.

Claims

Claim 1 has been amended to more clearly define the invention. Amended claim 1 recites a device for adjusting a current from the first bias current source to a first circuit to reduce the variation of the first circuit as a function of process, voltage and temperature, and the device includes a first transistor and a second transistor. Amended claim 1 further recites that the gate of the first transistor is coupled to the first gate reference voltage and the first node of the first transistor is coupled to the first bias current source, whereby the first transistor generates a current sensitive to the process, voltage and temperature variations. Amended claim 1 further recites that the gate and the first node of the second transistor is coupled to the first node of the first transistor and the first bias current source, whereby the second transistor adjusts a current proportional to the difference between the current generated by the first bias current source and the current from the first transistor.

The amendment to claim 1 is fully supported by the application as originally filed. In particular, support for "a device for adjusting a current from the first bias current source to a circuit to reduce the variation of the first circuit as a function of process, voltage and temperature" can be found, for example, in Paragraphs [0075] and [0077] and Fig. 17 of the original application; support for " a first transistor ..." can be found for example in Paragraphs [0075] and [0077] and Fig. 17 of the original application; support for " a second transistor ..." can be found, for example, on in Fig. 17 of the original application.

Applicant respectfully submits that "the second transistor adjusting a current proportional to the difference between the current generated by the first bias current source and the current from the first transistor" in claim 1 can be clearly read by a person skilled in the art from original Fig. 17.

Claim 2 has been cancelled without prejudice.

New dependent claims 19 to 21 have been added.

Claim 19 recites: "the structure of the gate of the first transistor includes a plurality of stripes." Support for new claim 19 can be found, for example, in original claim 3 and Paragraph [0075] of the original application.

Claim 20 recites: "the first transistor and the second transistor are NMOS transistors, the first node of the first transistor being a drain, the first node of the second transistor being a drain." Support for new claim 20 can be found, for example, in Fig. 17 of the original application.

Claim 21 recites: "the first circuit includes at least one of a delay cell, a delay lock loop (DLL), a phase lock loop (PLL), a charge pump, an Operational Amplifier, and an Input/Output pad." Support for new claim 21 can be found, for example, in Paragraph [0079] of the original application.

No new matter has been introduced by way of the amendments to the claims. Applicant respectfully requests the Examiner to enter the amendments described above.

Specification and Drawings

Applicant has added new Figures 19 to 24.

Fig. 19 illustrates the gate structure of a transistor included in the bias circuit of Fig. 17.

Figure 20 illustrates a basic delay lock loop (DLL) with the bias circuit of Fig. 17. Figure 21 illustrates a basic phase lock loop (PLL) with the bias circuit of Fig. 17. Fig. 22 illustrates a charge pump with the bias circuit of Fig. 17. Fig. 23 illustrates an Operational Amplifier with the bias circuit of Fig. 17. Fig. 24 illustrates an Input/Output pad with the bias circuit of Fig. 17. These circuits without having the bias circuit 600 are well known in the art.

A person of ordinary skill in the art could come up with these figures from the description as originally filed, for example, in Paragraphs [0075], [0077] and [0079], and originally filed claims 5 to 10.

Applicant respectfully requests the Examiner to enter these new figures.

Applicant has amended the specification to add new Paragraphs after Paragraph [0050] to briefly describe new Figures 19 to 24. No new matter has been introduced by way of the amendment.

Applicant has amended Paragraphs [0047] and [0050] to add minor changes. In particular, support for the amendment to Paragraph [0047] can be found in Paragraph [0073] of the original application; support for the amendment to Paragraph [0048] can be found in Paragraph [0074] of the original application; support for the amendment to Paragraph [0049] can be found in Paragraph [0076] and Fig. 17 of the original application. No new matter has been introduced by way of the amendment.

Applicant respectfully requests the Examiner to enter the amendments to the specification.

Objection Under 37 CFR §1.83(a)

Under Paragraph 1 of the Office Action, the Examiner objected to the drawings because "the gate is relatively short length relative to other gates in the CMOS circuit" (of claim 2) must be shown or the feature(s) cancelled from the claim(s).

Claim 2 has been cancelled without prejudice.

New claim 19 recites: "the structure of the gate of the first transistor includes a plurality of stripes." This feature is fully supported by the application as originally filed, and has been illustrated in new Fig. 19.

New claim 21 recites: "the first circuit (of claim 1) includes at least one of a delay cell, a delay lock loop (DLL), a phase lock loop (PLL), a charge pump, an operational Amplifier, and an Input/Output pad." This feature is fully supported by the application as originally filed, and has been illustrated by new Figs. 20 to 24.

It is respectfully submitted that the drawings show every feature of the invention specified in the claims.

Claim Rejections –35 USC §112

Under Paragraphs 2 to 3 of the Office Action, the Examiner rejected former claims 1 to 2 under 35 USC 112, first paragraph, as failing to comply with the written description requirement.

With respect to the rejection of former claim 1, the Examiner stated: "The specification fails to provide description of a gate size and structure to enhance its sensitivity to process, voltage and temperature variations thereby compensating the first bias current source for same".

Applicant respectfully submits that claim 1 has been amended to more clearly define the element "device" and complies with 35 USC 112, first paragraph.

With respect to the rejection of former claim 2, the Examiner stated that the specification also fails to provide description of "the gate is relatively short length relative to other gates in the CMOS circuit".

Claim 2 has been cancelled without prejudice.

Applicant respectfully requests the reconsideration and withdrawal of the rejections under 35 USC 112, first paragraph.

Claim Rejections –35 USC §102

Under Paragraphs 4 to 5 of the Office Action, the Examiner rejected former claim 1 under 35 USC 102 (e) as being anticipated by Sidiropoulos et al. (US Patent No. 6,573,779), hereinafter referred to as Sidiropoulos.

Applicant respectfully requests the reconsideration and withdrawal of the rejection in view of the cited reference, because claim 1 is patentable for reasons as set out below.

According to claim 1, a CMOS circuit includes a device for adjusting a current from a first bias current source to a circuit to reduce the variation of the first circuit as a function of process, voltage and temperature. The device includes a first transistor and a second transistor. The gate of the first transistor is coupled to a first gate reference voltage and the

first node of the first transistor is coupled to the first bias current source whereby the first transistor generates a current sensitive to process, voltage and temperature variations. The gate and the first node of the second transistor is coupled to the first node of the first transistor and the first bias current source whereby the second transistor adjusts a current proportional to the difference between the current generated by the first bias current source and the current from the first transistor.

The Examiner stated: "Sidiropoulos teaches all claimed features in Figs. 3 and 4, a CMOS circuit comprising: a first gate reference voltage (37); a first bias current source (Ibias); and a device (Mbs1) having its gate coupled to the first gate reference voltage (37), the device coupled in series with the first bias current source and having a gate size."

Sidiropoulos discloses a biasing circuit 42 (Fig. 4) connected to a reference generator 37 (Fig. 3). The biasing circuit 42 includes transistors Mbs1, Mbs2, Mbs3, Mbs4 and Mbs5. As acknowledged by the Examiner, the gate of the transistor Mbs1 is coupled to the reference generator 37.

However, the drain of the transistor Mbs1 is coupled to Ibias through the transistor Mbs2, while the gate and the drain of the transistor Mbs2 are coupled only to Ibias and not to both of Ibias **and** the drain of the transistor Mbs1. Sidiropoulos fails to disclose or suggest a combination of a first transistor and a second transistor, where the gate of the first transistor is coupled to the first gate reference voltage, the first node of the first transistor is coupled to the first bias current source, the gate and the first node of the second transistor is coupled to the first node of the first transistor and the first bias current source. Sidiropoulos neither discloses nor suggests a device having such combination of the first transistor and the second transistor for adjusting a current from the first bias current source to a first circuit to reduce the variation of the first circuit as a function of process, voltage and temperature.

Hence, Applicant respectfully submits the claim 1 is patentable in view of the cited reference.

Claim Rejections –35 USC §103

Under Paragraphs 6 to 7 of the Office Action, the Examiner rejected former claim 2 under 35 USC 103 (a) as being unpatentable in view of Sidiropoulos.

Claim 2 has been cancelled without prejudice.

Claims 19 to 21 now depend on claim 1 and include all limitations of claim 1. Accordingly, Applicant respectfully submits the claims 19 to 21 are patentable in view of the cited reference.

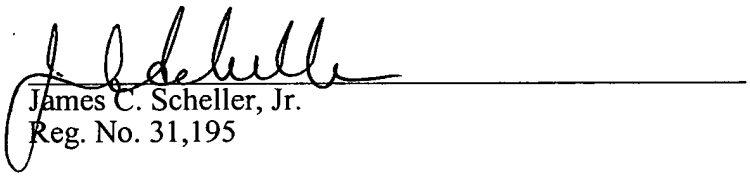
In view of the above amendments and arguments reconsideration and consequent allowance of claims is respectfully requested.

If any additional fees are required for this response, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 4/3, 2006



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